Microelectronics (ECCDLO5011)

Sem-V

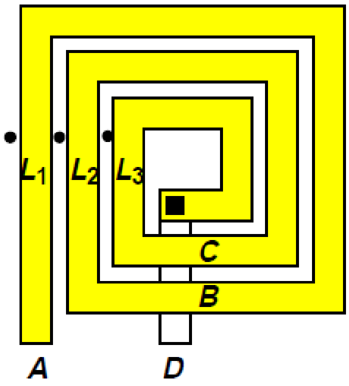
Q1-Q10:1M

Q11-Q15:2M

Q16-Q25:3M

1) Photo resist which is initially insoluble and becomes soluble after exposure to UV light is called
   a) Positive Photoresist
   b) Negative Photoresist
   c) Thermo photoresist
   d) Poly photoresist
2) In the mask layout green colour indicates
   a) p-diffusion
   b) metal contacts
   c) polysilicon
   d) n-diffusion
3) λ in MOSFET is
   a) Body effect coefficient
   b) channel length modulation coefficient.
   c) non ideality factor
   d) fitting parameter
4) The equation of current in Linear region for NMOS is
   a) $I_{DS}=K_N[(V_{GS}-V_{TN})V_{DS}-V_{DS}^2/2$
   b) $I_{DS}=K_P(V_{GS}-V_{TP})^2$
   c) $I_{DS}=K_N(V_{GS}-V_{TN})^2$
   d) $I_{DS}=K_N[(V_{GS}-V_{TN})V_{DS}$
5) For the two-transistor current source
   a) $I_o = \frac{(W/L)_2}{(W/L)_1} I_{ref}$
   b) $I_o = \frac{(W/L)_1}{(W/L)_2} I_{ref}$
   c) $I_{ref} = \frac{(W/L)_2}{(W/L)_1} I_o$
   d) $I_{ref} = (W/L)_2 I_o$
6) The output voltage of MOS Common Source with Resistive Load amplifier in triode region is
   a) $Vo = V_{DD}$
   b) $Vo = \frac{R_{ON}}{R_{ON}+R_D} V_{DD}$
   c) $V_O = V_{DD} - \frac{k_n}{2}(V_{GS} - V_{TH})^2 R_D$
   d) $V_O = \frac{k_n}{2}(V_{GS} - V_{TH})^2 R_D$

7) The overall inductance of the given inductor is



a) $L_1+L_2+L_3+M_{12}+M_{23}+M_{13}$
b) $M_{12}+M_{23}+M_{13}$
c) $L_1+L_2+L_3$
d) $M_1+M_2+M_3+L_{12}+L_{23}+L_{13}$

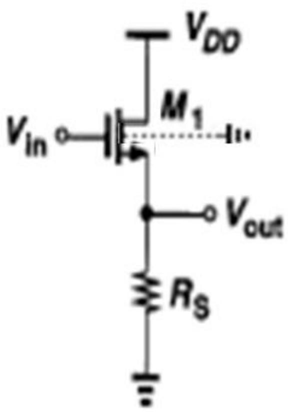
8) Conduction angle for class B power amplifier is
a) $\theta=180^0$
b) $\theta>180^0$
c) $\theta<180^0$
d) $0^0<\theta<180^0$

9) The CMRR for differential amplifier is given as
a) $CMRR = \frac{A_d}{A_C}$
b) $CMRR = \frac{A_C}{A_d}$
c) $CMRR = A_C A_d$
d) $CMRR = A_C$

10) In the MOS differential amplifier, the tail acts
a) Current source
b) Battery
c) Transistor
d) Diode

11) The equation of overdrive voltage in differential amplifier is(2M)
a) $\sqrt{I}/kn'(\frac{W}{L})$
b) $\sqrt{I}(\frac{W}{L})/kn'$
c) $Kn\sqrt{I}(\frac{W}{L})$
d) $Kn\sqrt{I}/(\frac{W}{L})$

12) For the given circuit the intrinsic gain is (2m)



a) $A_O = \frac{g_m}{(g_{m+}g_{mb})}$

b) $A_O = \frac{(g_{m+}g_{mb})}{(g_m)}$

c) $A_O = \frac{1}{\frac{1}{r_o}+g_m+g_{mb}}$

d) $A_O = \frac{1}{\frac{1}{r_o}(g_m+g_{mb})}$

13) The total capacitance between gate and source of MOS in saturation is given as(2M)

a) $C_{gs(T)} = \frac{1}{2}C_{ox}WL + C_{GS(overlap)}$
b) $C_{gs(T)} = \frac{2}{3}C_{ox}WL + C_{GS(overlap)}$
c) $C_{gs(T)} = C_{GS(overlap)}$
d) $C_{gs(T)} = 0.5C_{ox}WL$

14) For active load MOS differential amplifier, the differential gain is given as (2M)

a) $A_d = 2\sqrt{\frac{2K_n}{I_Q}}\frac{1}{\lambda_2+\lambda_4}$

b) $A_d = \sqrt{\frac{4K_n}{I_Q}}\frac{1}{\lambda_2+\lambda_4}$

c) $A_d = 2\sqrt{\frac{K_n}{I_Q}}\frac{1}{\lambda_2+\lambda_4}$

d) $A_d = 2\sqrt{\frac{3K_n}{I_Q}}\frac{1}{\lambda_2+\lambda_4}$

15) The problem of stacking caused by MOS active load in amplifiers can be avoided by(2M)
a) Cascoded amplifiers
b) Double cascaded
c) Folded cascode
d) Cascade amplifiers

16) Various measurements are made on an NMOS amplifier for which the drain resistor R_D is 20 kΩ. First, DC measurements show the voltage across the drain resistor, V_{RD}, to be 2 V and the

gate-to-source bias voltage to be 1.2 V. Then, ac measurements with small signals show the voltage gain to be −10 V/V. If the process transconductance parameter is 50μA/V^2, what is the MOSFET's W/L.?(3M)

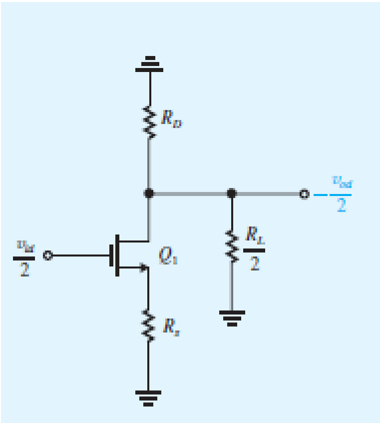
a)**25**

b)50

c)75

d)100

17) For the given circuit, the differential gain is (3M)



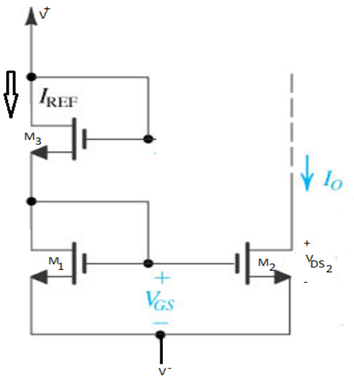
a) $A_d = \frac{R_{D//(\frac{R_L}{2})}}{\frac{1}{gm}+R_S}$

b) $A_d = \frac{R_{D//(\frac{R_L}{2})}}{\frac{1}{gm}}$

c) $A_d = \frac{R_{D//(\frac{R_L}{2})}}{R_S}$

d) $A_d = R_{D//(\frac{R_L}{2})}$

18) For the three transistor MOSFET current source having V$^+$=10V and V$^-$=2V. The transistor parameters are K_n=40μA/V^2, V_{TH}=1V and λ=0. The $(W/L)_2$ of M2 is Given that I_{ref}=0.25mA, I_o=0.1mA and V_{DS2}=0.85V. (3M)



a) 3.46

b) 0.235

c) 8.65

d) 4.25

19) Compare the output resistance of cascode MOSFET current source to two transistor current source. Assume $I_{ref}=I_O=100\mu A$ in both the circuits, $\lambda=0.01V^{-1}$ for the transistors and $g_m=0.5mA/V$.(3M)

a) 10times more
b) 5 times more
c) 20 times more
d) 500 times more

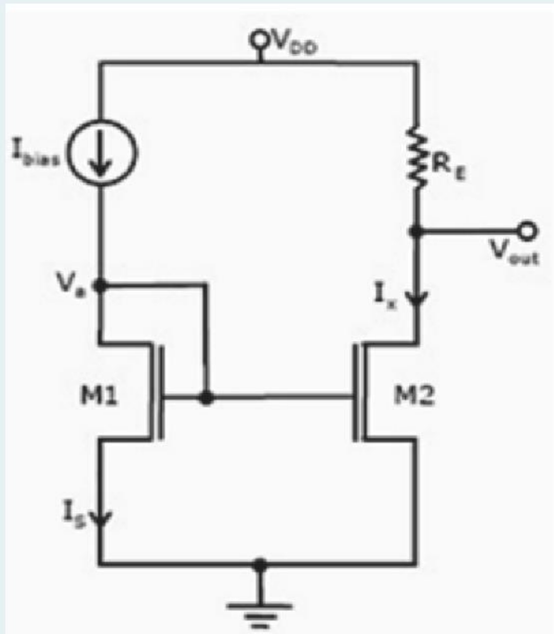
20) When the gate – to – source voltage (V_{GS}) of a MOSFET with threshold voltage of 400 mV, working in saturation is 900 mV, the drain current is observed to be 1 mA. Neglecting the channel width modulation effect and assuming that the MOSFET is operating at saturation, the drain current for an applied V_{GS} of 1400mV is (3M)

a) 0.5 mA
b) 4.0 mA
c) 2.0 mA
d) 3.5 mA

21) Consider the basic two transistor NMOS current source. the circuit parameters are V==5V, V-=-5V and Iref=0.250mA. The transistors parameters are $\lambda=0.02V^{-1}$, VTN=1V, Kn'=00.8mA/V2, If W/L=3 find I_O for V_{DS2}=3V. Give your answer in micro amperes.(3M)

a) 230
b) 252.8
c) 264
d) 224

22) For the circuit shown in fig transistors M1 and M2 are identical NMOS transistors. Assume that M2 is in saturation and the output is unloaded. The I_X is related to I_{bias}



as(3M)

a) $IX=Is-I_{bias}$
b) $IX=I_{bias}$
c) $IX=Is+I_{bias}$
d) $IX=I_{bias}-(V_{DD}-V_{out}/R_E)$

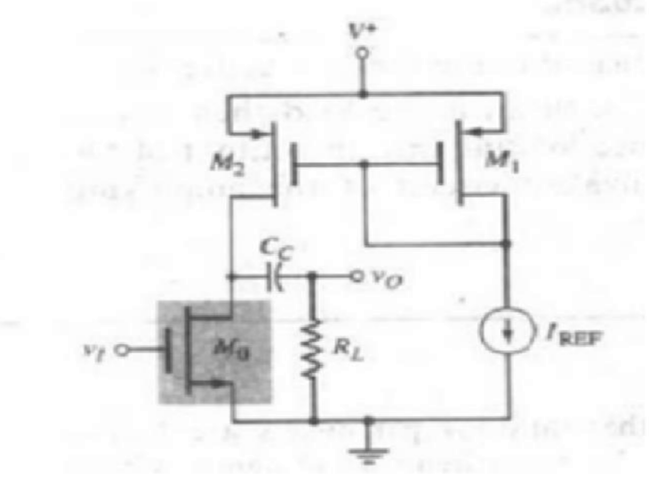
23) The current in an enhancement mode NMOS transistor biased in saturation mode was measured to be 1 mA at a drain source voltage of 5V. When the drain source voltage was increased to 6V while keeping gate source voltage same. The drain current increased to 1.02 mA. Assume that drain to source saturation voltage is much smaller than the applied drain source voltage. The channel length modulation parameter λ is (3M)

a) 0.011
b) 0.015
c) 0.022
d) 0.2

24) A depletion type N – channel MOSFET in biased in its linear region for use as a voltage-controlled resistor. Assume threshold voltage VTH =0.5V, VGS = 2.0V, VDS = 5V, W/L = 100, C_{OX} = 10^{-8} $F/cm2$ and μ_n = 800 $cm^2/V - s$. The value of the resistance of the voltage-controlled resistor (in Ω) is ___(3M)

a) 1K
b) 500
c) 900
d) 500.90

25) For the amplifier shown in fig. Assume M1 and M2 are matched. λn=λp=0.02V-1, V_{TN}=1V, V_{TP}=-1V, Kn=K_P=0.25mA/V^2. Let V^+=10V and Iref=0.4mA. what is the value of R_L that results in a voltage gain of one half the open circuit value.(3M)



a) 62.5k
b) 61.2
c) 71k
d) 70k